(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 064 614**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 82103228.1

(51) Int. Cl.³: H 01 L 29/08

(22) Date of filing: 16.04.82

(30) Priority: 30.04.81 JP 65951/81
30.04.81 JP 65966/81

(43) Date of publication of application:
17.11.82 Bulletin 82/46

(84) Designated Contracting States:
CH DE FR GB LI NL SE

(71) Applicant: TOKYO SHIBAURA DENKI KABUSHIKI KAISHA
72, Horikawa-cho Saiwai-ku
Kawasaki-shi Kanagawa-ken 210(JP)

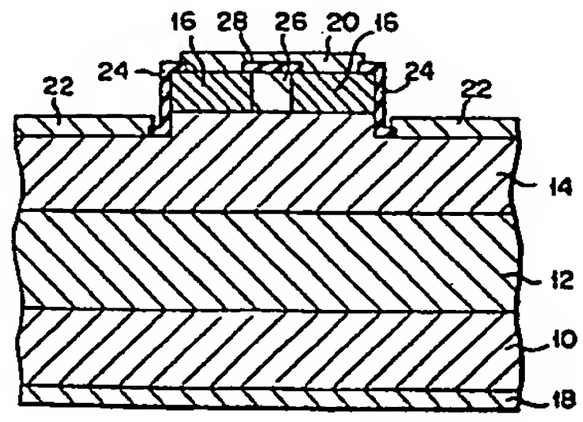
(72) Inventor: Makoto, Azuma
205 Nakakibogaoka
Asahi-ku Yokohama-shi(JP)

(74) Representative: PATENTANWÄLTE HENKEL - KERN - FEILER - HÄNZEL
Möhlstrasse 37
D-8000 München 80(DE)

(54) Improved emitter structure for semiconductor devices.

(57) A semiconductor device having a region (26) which becomes a depletion layer under a no bias condition and which is formed in each emitter layer (16) of a specified conductivity type to suppress the emitter current concentration. The emitter layers (16) are formed on the surface of a base layer (14) of the opposite conductivity type to be separate from one another or to be partially coupled to one another. The base layer (14) is formed on a semiconductor layer (10, 12) of at least a one layer structure.

FIG. 3



EP 0 064 614 A2

TITLE MODIFIED
see front page

Semiconductor device

The present invention relates to a semiconductor device and, more particularly, to an improved emitter structure which alleviates the current concentration by using a ballast inside the element to thereby reduce local thermal runaway.

The current distribution in a semiconductor element unit is generally not uniform. The current may concentrate on the part of the element unit which allows the easiest flow of current and thus may damage the element unit. This phenomenon will be more specifically described taking as examples a gate turn-off thyristor and transistors having a comb-shaped emitter structure and a multi-emitter structure.

A gate turn-off thyristor (to be referred to as a GTO for brevity hereinafter) is a four-layered semiconductor device, which is similar to a general thyristor in that the gate electrode is maintained at a positive potential to allow flow of a gate current and to trigger the device. The thyristor of the general type is turned off by commutating the main current through a commutation circuit. In contrast to this, the GTO is turned off by maintaining the gate electrode at a negative potential which causes negative current flow. Since the commutation circuit requires space and cost and renders the overall device complex in structure, the omission

of the commutation circuit provides a considerable advantage. When the devices' characteristics are considered, the turn-off time of the GTO is significantly shorter than that of the general thyristor, thus providing another advantage.

Fig. 1 is a sectional view of one element unit of a conventional GTO. Referring to Fig. 1, an n-type first base layer 12 is formed to be contiguous with a p-type first emitter layer 10 to form a p-n junction therewith. A p-type second base layer 14 is formed to be contiguous with the n-type first base layer 12 to form another p-n junction therewith. A mesa n-type second emitter layer 16 is formed to be contiguous with the p-type second base layer 14 to form still another p-n junction. An anode electrode 18, a cathode electrode 20 and a gate electrode 22 are formed as shown in Fig. 1. An insulation film 24 is formed to cover the exposed part of the p-n junction surrounding the mesa n-type second emitter layer 16. The GTO generally has a structure in which the second emitter layer 16 is divided into a plurality of parts in order to minimize the voltage drop, which is determined by the product of the gate current flowing through the second base layer 14 upon a turn-off operation, and the lateral resistance. Thus, an actual GTO would include a number of element units of the structure as shown in Fig. 1. A plurality of element units are arranged to operate in parallel to each other.

In the conventional GTO shown in Fig. 1, the current concentrates at a point which is farthest from the gate electrode 22 during a turn-off operation, that is, at the center of the second emitter layer 16. This is illustrated in Fig. 2, and will be described in more detail below. When a gate turn-off signal is applied to the gate electrode 22, that part of the second emitter layer 16 which is immediately adjacent to the gate electrode 22 is rendered nonconductive first. Thus,

the current is suppressed toward the center of the second emitter layer 16. As the turn-off operation proceeds and the nonconductive region expands, the current density increases near the center of the second emitter layer 16. When the conductive region is sufficiently decreased and restoring of the current becomes impossible, the GTO turns off one-dimensionally.

However, when the gate current flowing to the gate electrode decreases to the minimum value required to turn off the GTO during the turn-off operation, the GTO cannot complete the turn-off operation and will be damaged by the excessive thermal loss.

Conventional methods for preventing the current concentration at the second emitter layer 16 during the turn-off operation includes a method for adopting a second emitter layer 16 composed of a plurality of segments of a smaller width, and a method for increasing the impurity concentration of the second base layer 14 to thereby reduce the lateral resistance of the second base layer and to allow flow of the gate current which is sufficient to complete the turn-off operation. Furthermore, the gate-cathode voltage is increased during the turn-off operation to increase the drift electric field of the second base layer 14 so that the turn-off operation is facilitated. Although these methods alleviate the current concentration phenomenon to some extent, they fail to provide the optimal solution to the problem. This is attributable to the following fact. Although the anode current may be increased in correspondence with the increase in the gate current, the extent to which the gate current may be increased is limited due to the intrinsic impedance of the second base layer 14 and the gate-cathode junction reverse breakdown voltage.

The current concentration phenomenon will now be described with reference to the cases of transistors having either a comb-shaped emitter structure or

a multi-emitter structure.

In a transistor having a comb-shaped emitter structure or the multi-emitter structure with a plurality of independent emitters, currents of different values flow through the respective emitters. This is mainly attributable to the fact that it is difficult to obtain transistor elements of uniform characteristics due to the nonuniformity in the impurity diffusion during the manufacture of the transistors or to the nonuniform distribution of the substrate crystal defects during heat treatment. Especially with the comb-shaped emitter structure, the distances the currents flow differ from one element to another since the emitter electrodes interleave with the base electrodes. Because of this, the resistive component distribution determines the current distribution. At that part where a high current flows, the temperature rises proportional to the power consumption represented by the product of the collector voltage and the collector current. As the temperature rises, the base-emitter voltage is reduced and the current thus continuously increases. This positive feedback is repeated. When the temperature exceeds a critical temperature for maintaining the p-n junction, the transistor breaks down.

In order to solve this problem, according to the conventional method, a ballast resistor is incorporated in the emitter or the base. The resistance of this ballast resistor is set to be greater than the sum of the resistances of the other parts of the element, so that the current distribution may be made uniform. Although this method does not decrease the occupying area of the emitter and is excellent in terms of efficiency, it makes the manufacture of the device very difficult. In general, a ballast resistor is formed by selectively forming, on the electrode, a thin film containing metal atoms or a polycrystalline silicon layer in which an impurity is doped, and forming a

wiring electrode thereon. This process is complex in procedure and creates problems in that etching of the resistor layer becomes difficult and a weak adhesion exists between the metal and the resistor layer. In addition, the resistance of the ballast resistor is difficult to control. For example, in order to form a thin film resistor 5,000 Å thick on a rectangular electrode of 100 μm × 500 μm, the sheet resistance of the thin film becomes 10^6 ohms/square (Ω/□), if the resistance is set to 5Ω. It is extremely difficult to constantly maintain such a high sheet resistance, expecially since the interelement distribution of the emitter-collector saturation voltage VCE(sat) is degraded.

It is an object of the present invention to provide a semiconductor device with an improved emitter structure.

Another object of the present invention is to provide a semiconductor device which incorporates a ballast function inside the semiconductor device to make the current distribution inside an element unit uniform.

A further object of this invention is to provide a semiconductor device in which the current concentration may be reduced and local thermal runaway may be prevented.

The object may be achieved by a semiconductor device which comprises: a base layer of a first conductivity type which is formed on a semiconductor layer of at least one layer; emitter layers of a second conductivity type which are formed on a surface of the base layer so as to be separate from one another or to be partially coupled to one another; and a region which defines a depletion layer under a no bias condition and which is formed in each of the emitter layers so as to suppress the concentration of emitter currents.

According to the present invention, a region which defines a depletion layer under a no bias condition is formed in each emitter layer. Therefore, the current

in the emitter layer necessarily disperses, so that the current distribution becomes uniform and the local thermal runaway can be prevented.

According to another aspect of the present invention, a low impurity concentration region of a conductivity type the same as that of the emitter layer is formed at the center of the emitter layer, which is contiguous with the cathode electrode. Then, the depletion layer expands mainly into the low impurity concentration region because of the built-in voltage of the p-n junction formed by the base layer and the lower impurity concentration region inside the emitter layer. As a consequence, the carrier injection into the base layer from the low impurity concentration region is suppressed. The current in the emitter layer necessarily disperses and the threshold value for the breakdown due to current concentration increases.

By way of example and to make the description clearer, reference is made to the accompanying drawings, in which:

Fig. 1 is a partial sectional view of one element unit of a conventional gate turn-off thyristor;

Fig. 2 is a view showing the current concentration in the element unit shown in Fig. 1;

Fig. 3 is a partial sectional view showing one element unit of a gate turn-off thyristor according to a first embodiment of the present invention;

Fig. 4 is a view showing the pattern of an n -type layer 26 of the element unit shown in Fig. 3;

Fig. 5 is a view showing the dispersion of the current in the element unit shown in Fig. 3;

Fig. 6 is a partial sectional view of a modification of the first embodiment shown in Fig. 3;

Fig. 7 is a view showing the pattern of the n^--type layer 26 according to the modification shown in Fig. 6;

Fig. 8 is a partial sectional view of one element unit of a transistor according to a second embodiment

of the present invention;

Fig. 9 is a view showing the pattern of an n^--type layer 52 of the element unit shown in Fig. 8;

Fig. 10 is a view showing another pattern of the n^--type layer 52 of the element unit shown in Fig. 8; and

Fig. 11 is a partial sectional view of a modification of the second embodiment of the present invention.

Fig. 3 shows the structure, in section, of one element unit of a gate turn-off thyristor (to be referred to as a GTO for brevity hereinafter) according to the first embodiment of the present invention. The same reference numerals in Fig. 3 denote the same parts as in Fig. 1, and the detailed description thereof will be omitted. The element unit shown in Fig. 3 differs from that shown in Fig. 1 in that a low impurity concentration layer of the same conductivity type as that of the second emitter layer 16, that is, an n^--type layer 26 is formed in the second emitter layer 16. In this embodiment, an insulation film 28 covers the n^--type layer 26, and the cathode electrode 20 covers the insulation film 28. The n^--type layer 26 is formed in the center of the second emitter layer 16 an equal distance from the periphery of the second emitter layer 16, as seen from the pattern of Fig. 4.

The effects of the first embodiment of the present invention will now be described. The GTO of this embodiment is characterized in that the n^--type layer 26 forms a region to completely cut off the current in the second emitter layer 16, so that the local current concentration, which occurs during the turn-off operation, may be minimized. The impurity concentration of the second base layer 14 in the vicinity of the second emitter layer 16 is generally about 10^{17} to 10^{18} cm^{-3}. Therefore, if the impurity concentration of the n^--type layer 26 is sufficiently lower than this value, the p-n junction formed by the second base layer 14 and the

n^--type layer 26 may be approximated by a step junction. The built-in voltage of the step junction may be easily determined according to "Physics and Technology of Semiconductor Devices" by A.S. Groove, John Wiley and Sons, Inc. Thus, the built-in voltage ϕT may be expressed by equation (1) below:

$$\phi T = (KT/q)\ell n[(NA \cdot ND)/ni^2] \quad \ldots (1)$$

where K is the Boltsman constant, T is the junction temperature, q is the electron charge, NA is the acceptor concentration of the second base layer 14, ND is the donor concentration of the n^--type layer 26, and ni is the intrinsic concentration. The width W of the depletion layer extending into the n^--type layer 26 under zero bias conditions may be expressed by equation (2) below:

$$W = \sqrt{2\varepsilon s/qND \cdot \phi T} \quad \ldots (2)$$

where εs is the dielectric constant. Using relations (1) and (2) above, the impurity concentration ND of the n^--type layer 26 and the width W of the depletion layer extending therein may be determined.

When the impurity concentration ND is varied under the conditions of NA = 10^{17} cm^{-3} and NA = 10^{18} cm^{-3}, the built-in voltages ϕT and the widths W may be obtained in case of silicon as shown in Table 1 below:

Table 1

NA (cm^{-3})	ND (cm^{-3})	ϕT (V)	W (μm)
1×10^{17}	1×10^{15}	0.691	0.96
	1×10^{14}	0.632	2.90
	1×10^{13}	0.572	8.72
1×10^{18}	1×10^{15}	0.751	1.00
	1×10^{14}	0.691	3.03
	1×10^{13}	0.632	9.16

As may be seen from the table above, the lower the impurity concentration ND, the greater the increase in the width W and the greater the increase in the current cut-off capacity. When the impurity concentration is 1×10^{15} cm^{-3} or more, the width becomes 1 μm or less, extremely reducing the effects of the present invention. Fig. 5 shows the dispersion of the concentrated current according to this embodiment.

The GTO of this embodiment may be manufactured by the procedure to be described below. A semiconductor wafer for the first base layer 12 has a specific resistivity of 10 to 300 Ω·cm, has a thickness of 0.2 to 1.2 mm, and contains an n-type impurity such as phosphorus. Although the specific resistivity and the thickness of the semiconductor wafer may be selected within the relatively wider ranges as given above, they must be appropriately selected according to the off-state voltage rating of the GTO. The off-state voltage rating obtainable with the impurity concentration and the width in the ranges as given above is within the range of 300 to 6,000 V. A p-type impurity such as gallium or boron is diffused from both major surfaces of the semiconductor wafer to form a first emitter layer 10 and a second base layer 14 having a surface impurity concentration of 10^{17} to 10^{19} cm^{-3} and a thickness of 30 to 80 μm. A three-layered pnp structure is thus obtained. Next, an n^--type epitaxial layer of an impurity concentration of 10^{15} cm^{-3} or less and a thickness of 2 to 30 μm is formed on the second base layer 14. After depositing a masking material of n conductivity type such as a thermal oxide film on each surface of the wafer, a contact hole is formed in correspondence with the high impurity concentration emitter part by lithography. An n-type impurity such as $POc\ell_3$ or PH_3 is diffused through the contact hole to form a second emitter layer 16.

After selectively forming a contact hole in the

part of the second emitter layer 20 corresponding to the gate electrode by photolithography, the epitaxial layer is removed by etching so that the underlying part of the second base layer 14 may be exposed. The surface part of the n^--type layer 26 exposing the second base layer 14 is covered by an insulation film 28. The effects of the present invention may be achieved even if this step is omitted. Thereafter, an insulation film for passivation is formed on the exposed surface of the p-n junction consisting of an n-type emitter and a p-type base. Then, the cathode, gate and anode electrodes are formed according to methods well known in the art.

The concrete data of the embodiment as described above will now be given. The semiconductor wafer has a specific resistivity of 25 Ω·cm and a thickness of 250 μm. The p-type impurity doped layer has a surface impurity concentration of 6×10^{17} cm^{-3} and a thickness of 45 μm. The second emitter layer has a surface impurity concentration of 5×10^{20} cm^{-3} and a thickness of 6 μm. The n^--type epitaxial layer has an average impurity concentration of 2×10^{14} cm^{-3} and a thickness of 5 μm. The width of the depletion layer extending into the epitaxial layer is approximately 5 μm. It was found that the GTO having the epitaxial layer as described above at the center, can control a current having a value of 1.8 to 2.0 times the value of the current that is controllable with the GTO of conventional structure.

In the first embodiment as described above, the n^--type layer 26 forms a region which becomes a depletion layer under a no bias condition so as to suppress the current concentration at the second emitter layer 16. However, a p^--type layer 30 may alternatively be formed as shown in Fig. 6. In this case, the p^--type layer 30 is filled with the depletion layer which extends not from the bottom surface but from the side surfaces. However, with this p^--type layer 30, the emitter current

may be dispersed as in the case of the first embodiment. In order to manufacture a GTO of this strucuture, a p^--type epitaxial layer is grown in place of the n^--type epitaxial layer of the first embodiment.

When the surface impurity concentration of the second emitter layer 16 is 6×10^{20} cm^{-3}, the emitter depth is 5 μm, the thickness of the p^--type epitaxial layer is 5 μm, and the surface impurity concentration of the second base layer 14 is 1×10^{17} cm^{-3}; the donor concentration ND of the second emitter layer 16, the acceptor concentration NA of the p^--type layer 30 and the width W of the p^--type layer 30 may be obtained as in Table 2 below:

Table 2

Distance from surface (μm)	ND (cm^{-3})	NA (cm^{-3})	W (μm)
0	6×10^{20}	1×10^{13}	10.3
1	5.8×10^{20}	1×10^{13}	10.3
2	4.2×10^{20}	3×10^{13}	6.0
3	1.4×10^{20}	3×10^{14}	2.0
4	1.1×10^{19}	1×10^{16}	0.7

As may be seen from Table 2 above, if the width of the p^--type layer 30 is 10.3 μm, that part of the p^--type layer 30 which is 1 μm from the surface is filled with the depletion layer. In other words, the current does not flow in this part. If the width of the p^--type layer 30 is set to be 10.3 μm or less, a thicker layer portion is filled with the depletion layer. Then, the injection from the sides of the emitter is suppressed correspondingly, and the current cut-off capacity increases. From the standpoints of the precision in the current pattern processing and the lateral

diffusion precision during the formation of the emitter region, it is not realistic to set the width of the p^--type layer 30 to 1 μm or less. Since the acceptor concentration NA of the p^--type layer 30 is 1×10^{15} cm^{-3}, if the width W is 1 μm, the maximum value of the average impurity concentration of the p^--type layer 30 is 10^{15} cm^{-3}.

According to this embodiment, the current may be cut off at any portion of the second emitter layer 16. Since the current concentrates at that part of the second emitter layer 16 farthest from the gate during the turn-off operation, that is, at the center of the second emitter layer 16, the current dispersing effects are best facilitated if the depletion region is located at the center of the emitter as in the former embodiment. However, if the second emitter layer is of rectangular shape, carriers are observed by an infrared ray microscope to concentrate at the center (along the width) of the emitter first, then concentrate in the longitudinal direction, and finally concentrate in a spot of 200 to 300 μm in diameter during the turn-off operation. Therefore, improved effects may be obtained if another depletion layer is formed in addition to that formed at the center of the emitter, depending upon the shape of the emitter. For example, in the embodiment shown in Fig 3, the pattern of the n^--type layer 26 in the second emitter layer 16 may be as shown in Fig. 7. Similar modifications may be made if the p^--type layer 30 is formed in place of the n^--type layer 26. Although this embodiment is described with reference to a mesa GTO, this embodiment may similarly be applicable to a planar GTO.

Furthermore, the selective ion implantation method may be used to form a region which becomes a depletion layer under a no bias condition inside the second emitter layer 16 though the epitaxial growth method is used in the embodiment as described above.

To summarize, the embodiment has a region which becomes a depletion layer under a no bias condition inside the second emitter layer 16, obtained by dividing the original layer into a plurality of regions. A GTO is thereby provided wherein the current concentration inside the second emitter layer 16, during the turn-off operation, may be effectively suppressed and the switching operation may be performed with excellent reliability.

Fig. 8 is a sectional view of one element unit of a transistor according to the second embodiment of the present invention. In this embodiment, a collector layer 40 comprises an n^+-type layer 40_1 of high impurity concentration and an n-type layer 40_2 of an impurity concentration significantly lower than that of the layer 40_1. A p-type base layer 42 is formed on the n-type layer 40_2 to form a p-n junction therewith. An n^+-type emitter layer 44 is formed in the surface layer of the p-type base layer 42 to provide a p-n junction therewith. A collector electrode 46, an emitter electrode 48 and a base electrode 50 are formed in ohmic contact with the collector layer 40_1, the emitter layer 44 and the base layer 42, respectively. An n^--type layer 52 of low impurity concentration is formed in the emitter layer 44 so as to suppress the concentration of current. Insulation films 54 and 56 are formed on the surface of the n^--type layer 52 and the base-emitter junction surface. In an actual transistor, a number of these elements are formed with common collectors and bases, and these elements are operated in parallel with each other.

The n^+-type layer 40_1 of the collector layer 40 has a surface impurity concentration of 10^{19} to 10^{21} cm^{-3} if it is formed by diffusion using the n-type layer 40_2 as a substrate. The n^+-type layer 40_1, however, generally has an average impurity concentration of 10^{18} to 10^{21} cm^{-3} if a uniformly doped substrate is used. The average

impurity concentration of the n-type layer 40_2 is, in general, determined by the rated collector-base voltage, the rated collector-emitter voltage or the rated current amplification factor. However, the n-type layer 40_2 generally has an average impurity concentration of 10^{13} to 10^{16} cm^{-3} and a thickness of several to 300 μm. The base layer 42 is formed by the epitaxial growth method or diffusion of an impurity. The base layer 42 has an average impurity concentration of about 10^{14} to 10^{17} cm^{-3} although it significantly changes depending upon the application of the transistor. This embodiment is characterized in that the n^--type layer 52 is formed in the emitter layer 44 to be contiguous with the base layer 42. The emitter layer 44 has an impurity concentration of 10^{18} cm^{-3} or more as in the case of conventional emitters. However, the n^--type impurity layer 52 has an impurity concentration of 10^{15} cm^{-3} which is significantly lower than that of the emitter layer 44, and is formed by the epitaxial growth method or ion implantation.

The planar arrangement of the n^--type layer 52 differs depending upon the application of the transistor. In the case of a switching transistor, the main problem is the increase in the area of safe operation under reverse bias. Since the current concentrates at the center of the emitter, the n^--type layer 52 is formed at the center of the emitter layer 44 at substantially an equal distance from the periphery thereof, as shown in Fig. 9, to attain the current dispersion effects. In a general transistor, it is also effective to form the n^--type layer 52 at the center of the emitter where the current tends to concentrate in order to increase the area of safe operation under forward bias. In a transistor, the main elements of which are formed by implantation of impurities to low concentrations, the current tends to concentrate near the base electrode. In this case, the n^--type layer 52 may be formed in the

region of the emitter layer 44 which is close to the base electrode as shown in Fig. 10. The current density is thereby decreased, and the current amplification factor may be increased. In order to facilitate the effects of the present invention, the insulation film 54 of, for example, SiO_2 or Si_3N_4 is formed on the exposed surface of the n^--type layer 52, and the emitter electrode 48 covers the insulation film 54. However, this insulation film 54 need not always be used.

The transistor of the second embodiment of the present invention may be manufactured according to the procedure to be described below. Since the formation of the collector and base regions is known to those skilled in the art, the description of it will be omitted. An n-type epitaxial layer having an average impurity concentration of 10^{15} cm^{-3} or less and a thickness of 2 to 30 micrometers is formed on a semiconductor wafer on which is already formed the base layer 42. After depositing an n-type masking material such as a thermal oxide film on the surface of the epitaxial layer, a high impurity concentration part is selectively etched to form a contact hole by known photolithography. An n-type impurity such as $POCl_3$ or PH_3 is doped through this contact hole to form the emitter layer 44. A p-type impurity is selectively doped in the part which corresponds to the base region when the structure is viewed from the top in a similar manner. The p-type impurity is doped to a concentration of 10^{17} cm^{-3} or more and to a depth to completely cover the epitaxial layer. The exposed surface of the n-type impurity layer is covered by an insulation film of SiO_2 or Si_3N_4. However, this particular step may be omitted. The subsequent steps, that is, the passivation of the p-n junctions and formation of the electrodes are known to those skilled in the art, and the description of them will therefore be omitted.

The effects of the second embodiment will now be

described. In conventional transistors, the distribution of the current flowing through the emitter is made uniform by a ballast resistor which is externally attached to the semiconductor device. In contrast to this, in the transistor of this embodiment, the n^--type layer 52 for preventing the current concentration is formed inside the semiconductor device, so that the current distribution may be made uniform. In comparison with the average impurity concentration of 10^{15} cm^{-3} or less of the n^--type layer 52 which is relatively low, the base layer 42 near the layer 52 has an impurity concentration of 10^{17} cm^{-3}. Therefore, the p-n junction formed by the n^--type layer 52 and the base layer 42 may be approximated by a step junction. The built-in voltage of the step junction may be easily determined according to "Physics and Technology of Semiconductor Devices" by A.S. Groove, John Wiley and Sons, Inc. as described above. Thus, the built-in voltage ϕT may be expressed by equation (3) below:

$$\phi T = (KT/q)\ell n[(NA \cdot ND)/ni^2] \quad \ldots (3)$$

where K is the Boltsman constant, T is the junction temperature, q is the electron charge, NA is the acceptor concentration of the base layer 42 near the emitter, ND is the donor concentration of the n^--type layer 52, and ni is the intrinsic concentration. The width W of the depletion layer extending into the n^--type layer 52 under a zero bias condition may be expressed by equation (4) below:

$$W = \sqrt{2\varepsilon s/qND \cdot \phi T} \quad \ldots (4)$$

where εs is the dielectric constant. Using relations (3) and (4) above, the impurity concentration ND of the n^--type layer 52 and the width W of the depletion layer extending therein may be determined.

When the acceptor concentration NA is 10^{17} cm^{-3}, the relationship of the impurity concentrations ND, the built-in voltages ϕT and the widths W may be obtained as shown in Table 1 above.

As can be seen from the table above, the lower the impurity concentration ND, the greater the increase in the width W and the greater the increase in the current cut-off capacity. When the impurity concentration is 1×10^{15} cm^{-3} or more, the width becomes 1 micrometer or less, extremely reducing the effects of the present invention.

The concrete data for the second embodiment of the present invention will now be given. The n-type layer 40_2 of the collector has a specific resistivity of 20 Ω·cm and a thickness of 50 micrometers. The p-type base layer 42 has a surface impurity concentration of 4×10^{17} cm^{-3} and a thickness of 12 micrometers. The emitter layer 44 has a surface impurity concentration of 5×10^{20} cm^{-3} and a thickness of 5 micrometers. The n^--type layer 52 as the epitaxial layer, has an average impurity concentration of 3.4×10^{13} cm^{-3} and a thickness of 5 micrometers. The width of the depletion layer extending into the n^--type layer 52 is about 5 micrometers. With a transistor in which the n^--type layer 52 is located at the center of the emitter layer 44 as in Fig. 9, the secondary breakdown voltage under forward bias is 1.2 to 1.4 times greater than that obtainable with a transistor of the conventional structure, the allowable current of the reverse bias being 1.8 to 2.0 times greater than that obtainable with the transistor of the conventional structure, and the current amplification factor hFE is 1.5 to 2.0 times greater than that obtainable with the transistor of the conventional structure.

In the second embodiment described above, a low impurity concentration layer, having an impurity which is the same conductivity type as that of the emitter layer, is used as a region which becomes a depletion layer under a no bias condition. However, similar effects may also be obtained when a low impurity concentration layer of opposite conductivity type,

that is, a p^--type layer 58 is formed in the emitter layer 44. In the embodiment shown in Fig. 8, the n^--type layer 52 exhibits the current cut-off effects owing to the depletion layer extending from the bottom surface. In contrast to this, in the embodiment shown in Fig. 11, the p^--type layer 58 exhibits the current cut-off effect owing to the depletion layer extending from the sides thereof.

With reference to Fig. 11, assume that the p^--type layer 58 is formed by the epitaxial growth method, has a thickness of 5 micrometers, and acceptor concentrations NA of various values. The emitter layer 44 is formed by ion implantation, has a thickness of 5 micrometers, and donor concentrations ND of various values. The base layer 42 has a surface impurity concentration of 1×10^{17} cm^{-3}. The depths from the surface and the widths W of the depletion layer extending in the p^--type layer 58 at each depth are obtained as shown in Table 2 above.

As may be seen from Table 2 above, if the width of the p^--type layer 58 is 10.3 micrometers, that part of the p^--type layer 58 which is 1 micrometer from the surface is filled with the depletion layer. In other words, the electron injection from the emitter layer 44 does not occur and the current does not flow into this part. If the width of the p^--type layer 58 is set to be 10.3 micrometers or less, a thicker layer portion is from the sides of the emitter is suppressed correspondingly, and the current cut-off capacity increases. From the standpoints of current pattern processing precision and lateral diffusion precision during the formation of the emitter region, it is not realistic to set the width of the p^--type layer 58 to 1 micrometer or less. Since the acceptor concentration NA of the p^--type layer 58 is 1×10^{15} cm^{-3} if the width W is 1 micrometer, the maximum value for the average impurity concentration of the p^--type layer 58 is 10^{15} cm^{-3}.

The embodiments of the present invention have been described with reference to planar transistors. However, similar effects may be obtained when the present invention is applied to mesa multi-emitter transistors.

In summary, according to the embodiments of the present invention, the comb-shaped emitter or multi-emitter of the transistor is improved to incorporate the ballast function inside the element, so that the area of safe operation of the transistor may be widened and the current amplification factor may be increased.

The present invention is not limited to the particular embodiments described above, and various changes and modifications may be made within the spirit and scope of the present invention.

Claims:

1. A semiconductor device having a semiconductor substrate of at least one layer, a base layer of a first conductivity type which is formed on said semiconductor substrate, and a plurality of emitter layers of a second conductivity type which are formed on a surface of said base layer, characterized in that a region (26, 30, 52, 58) which becomes a depletion layer under a no bias condition is formed in each of said emitter layers (16, 44) so as to suppress concentration of emitter currents.

2. A semiconductor device according to claim 1, characterized in that said base layer (14) is formed on another base layer (12) of said second conductivity type formed on another emitter layer (10) of said first conductivity type.

3. A semiconductor device according to claim 1, characterized in that said base layer (42) is formed on said semiconductor substrate including a collector layer (40) of said second conductivity type.

4. A semiconductor device according to claim 1 or 2 or 3, characterized in that said region (26, 30, 52, 58) is formed at a center of said emitter layer.

5. A semiconductor device according to claim 1 or 3, characterized in that said region (26, 30, 52, 58) is positioned an equal distance from the periphery of said emitter layer.

6. A semiconductor device according to claim 1, characterized in that said region (26, 30, 52, 58) comprises a low impurity concentration semiconductor layer of said first conductivity type.

7. A semiconductor device according to claim 1, characterized in that said region (26, 30, 52, 58) comprises a low impurity concentration semiconductor layer of said second conductivity type.

FIG. 1

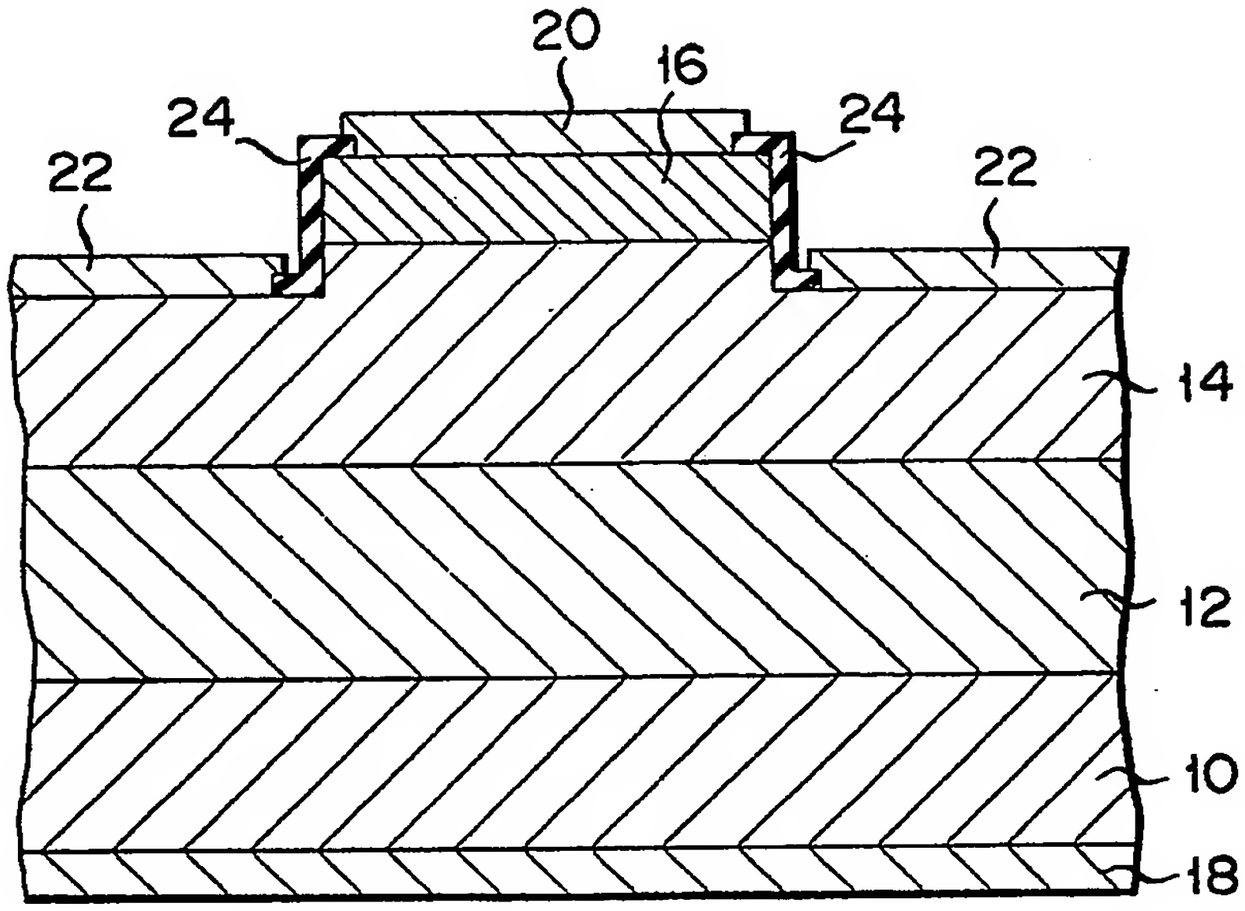
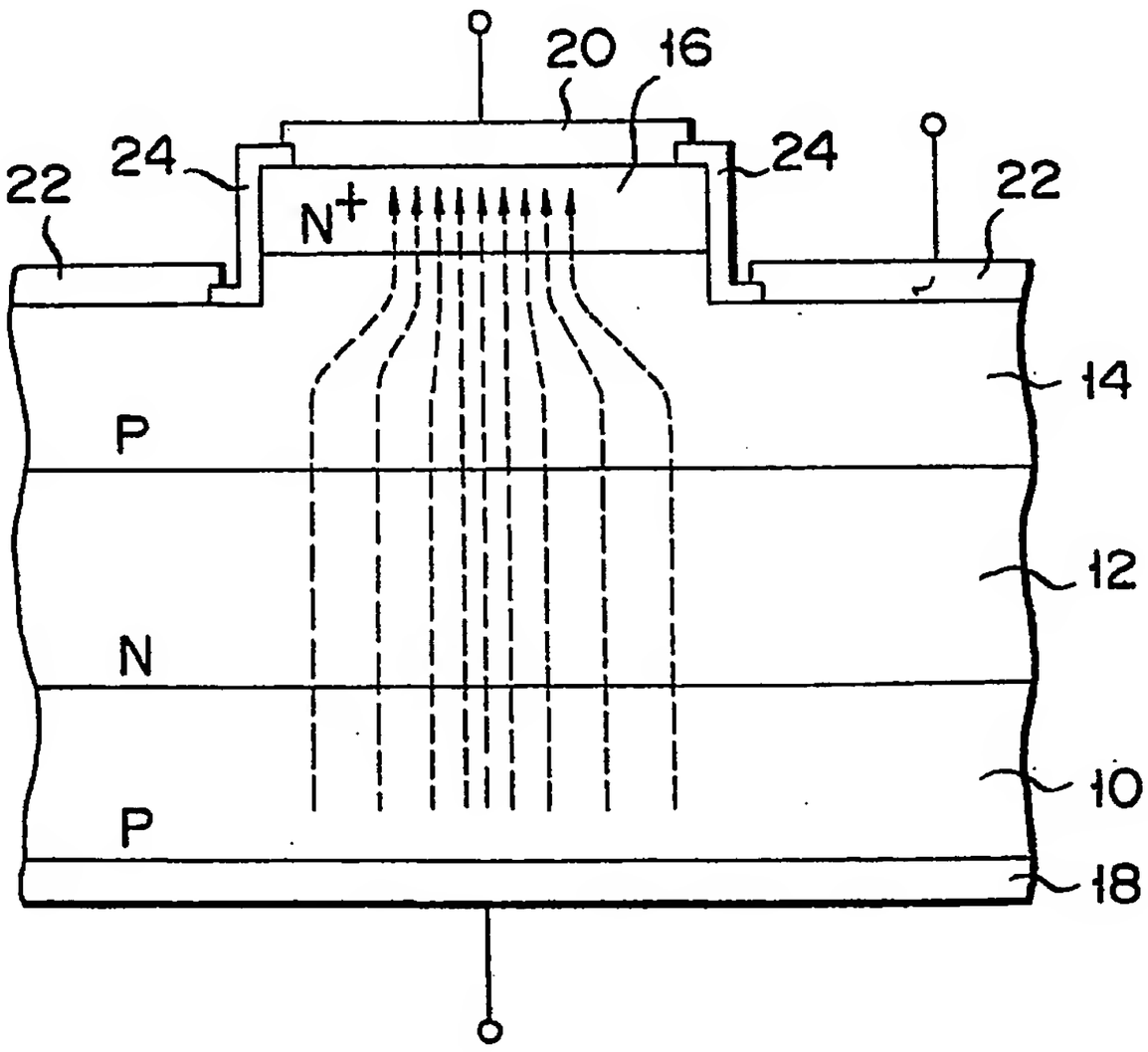


FIG. 2



0064614

FIG. 3

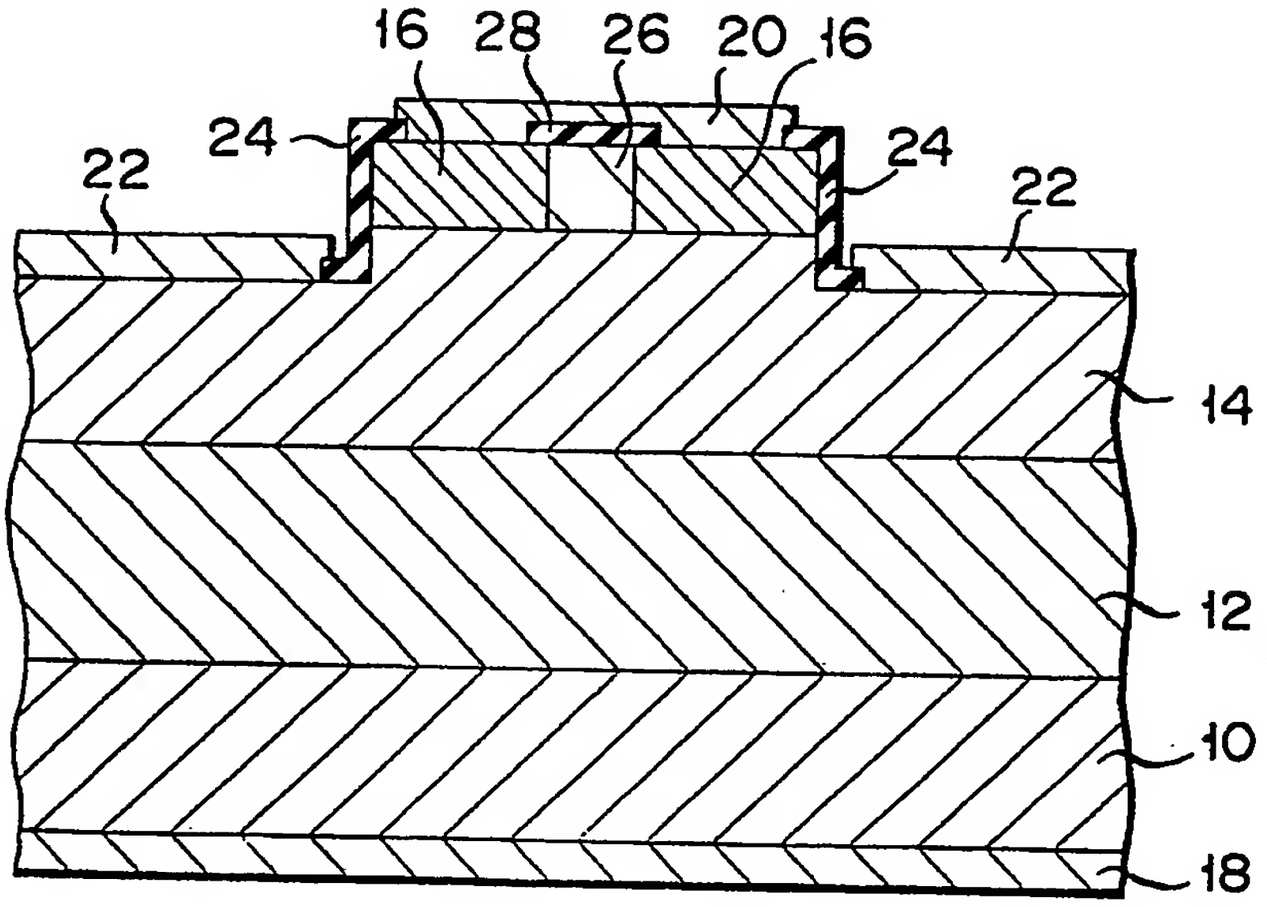


FIG. 4

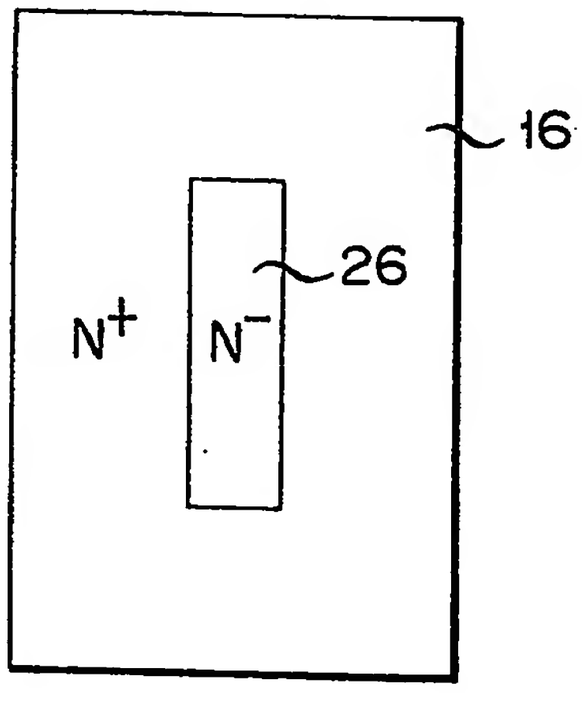


FIG. 5

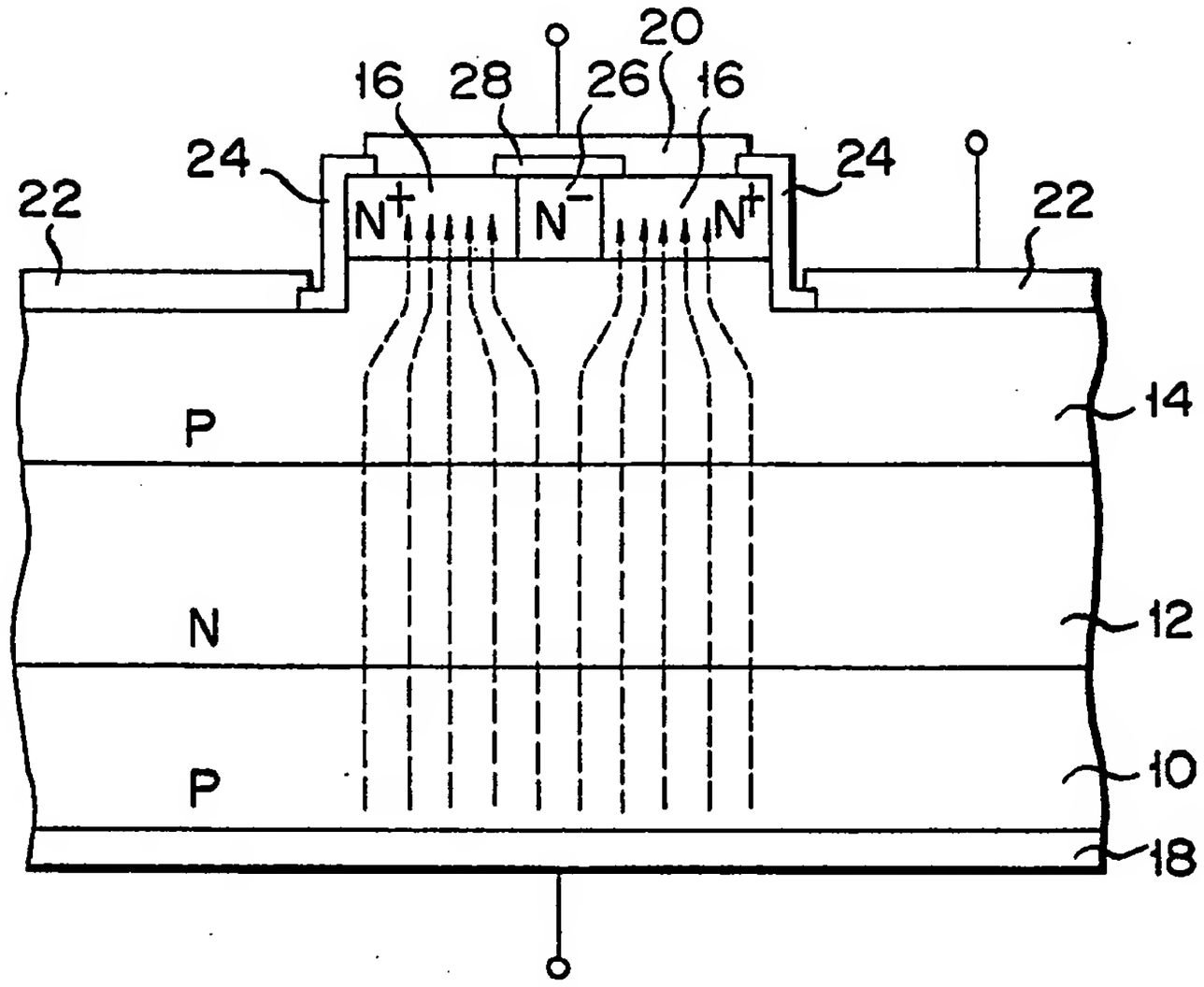

20
16
28
26
16
24
24
22
22
N^+
N^-
N^+
14
P
N
12
P
10
18

FIG. 6

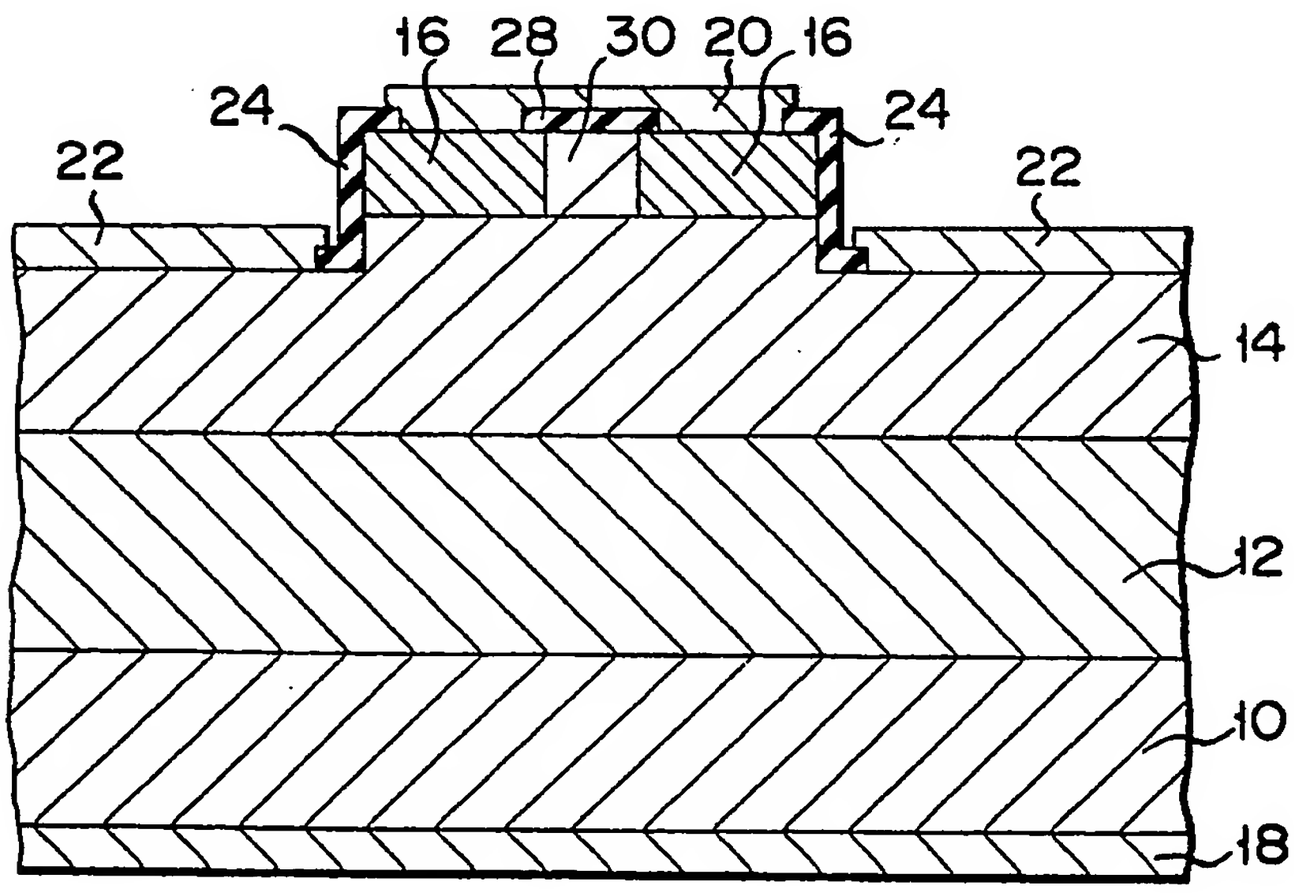

16
28
30
20
16
24
24
22
22
14
12
10
18

FIG. 7

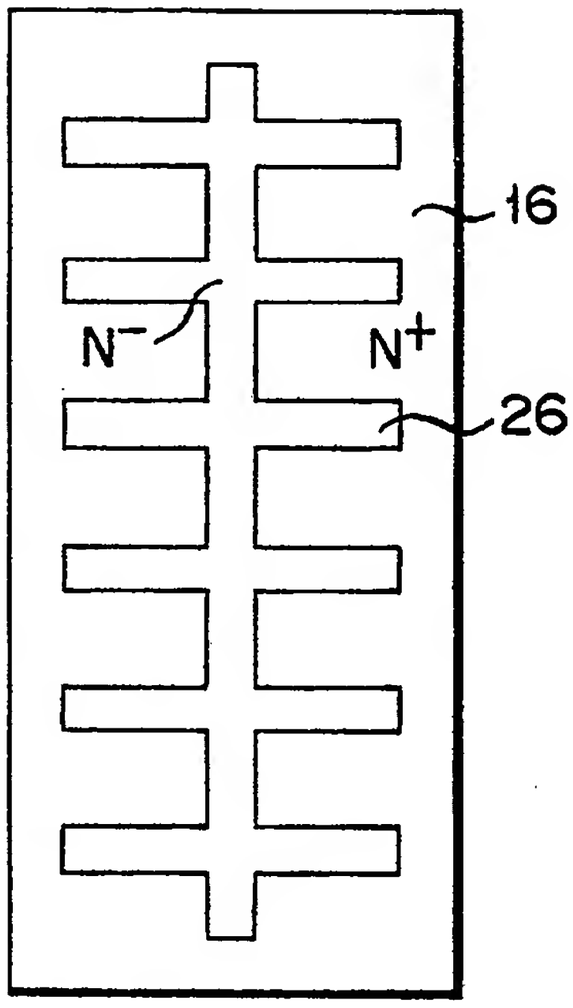


FIG. 8

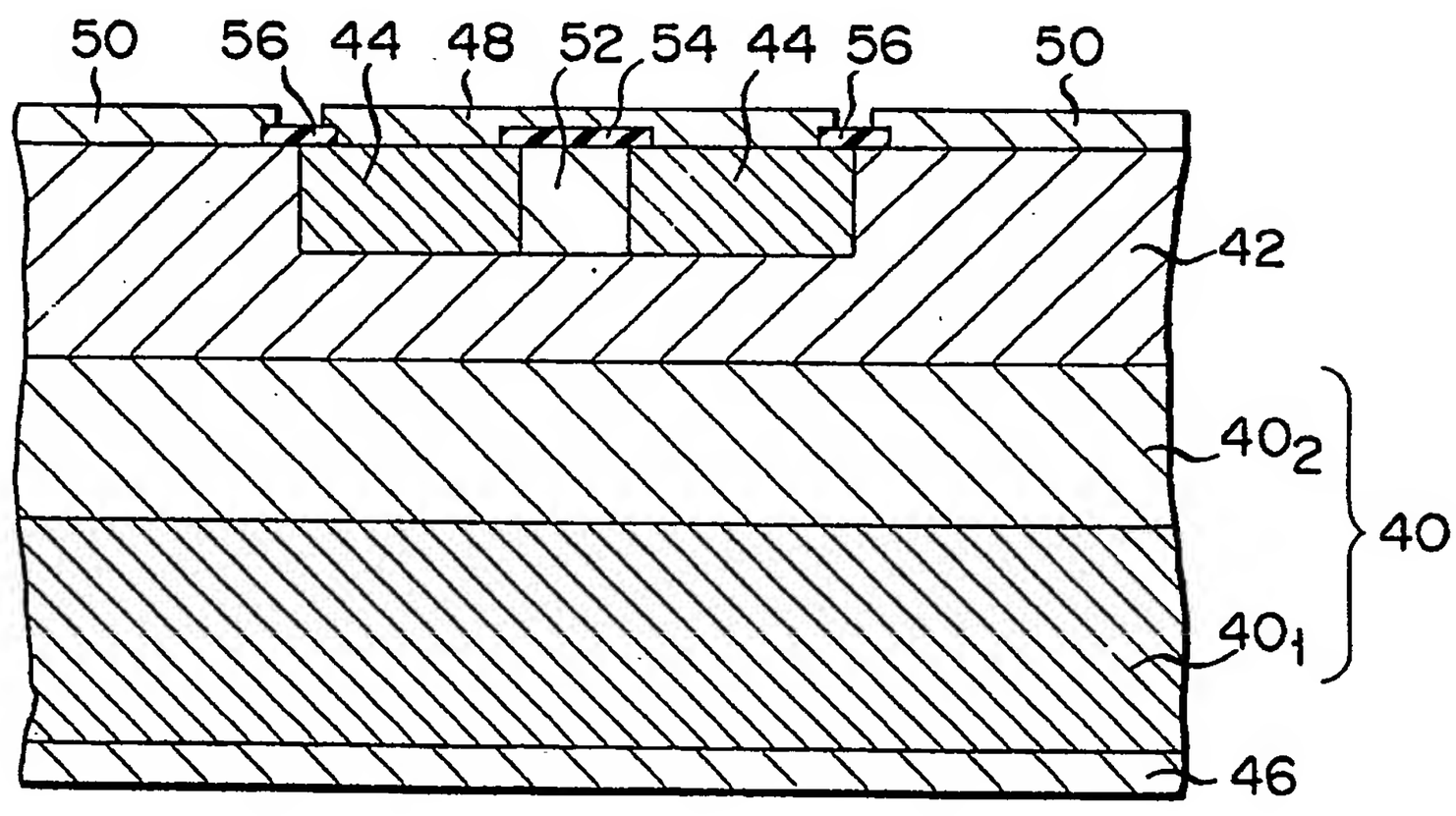


FIG. 9

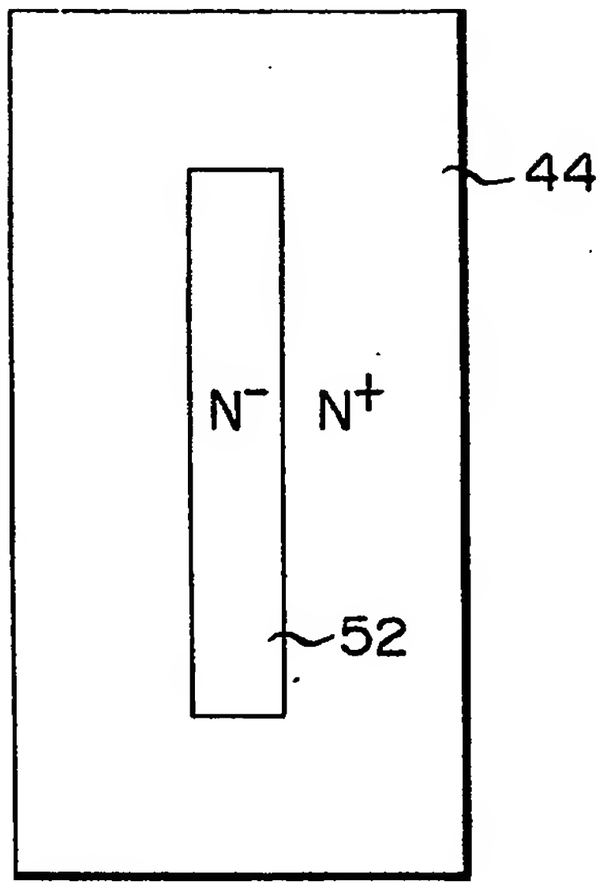


FIG. 10

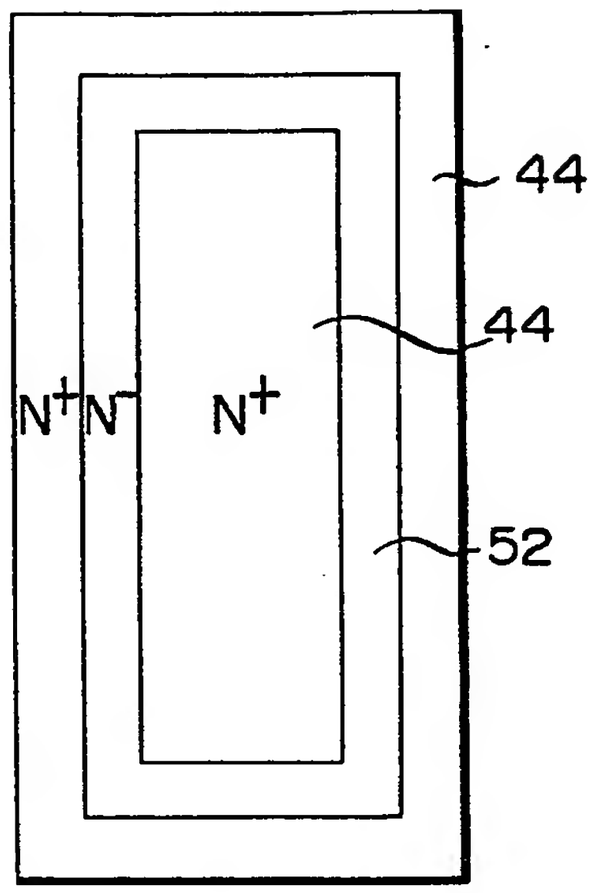


FIG. 11